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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/921,423	Applicant(s) THAKUR ET AL.	
	Examiner Johannes P Mondt	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2002*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

Amendment B filed 4/23/02 has been entered as Paper No. 5. Please be referred to "Response to Arguments" for the examiner's response to Applicant's "Remarks". The examiner has considered Amendment B prior to this Office Action.

Drawings

The examiner approves the changes in the drawings submitted by Applicant together with Amendment B.

Response to Arguments

1. *With regard to the traverse of the rejection under U.S.C. 103(a) of claims 1-10 and 13,* the examiner had given as motivation for the selection of boro-phosphosilicate glass for the nonconductive oxide with first etch rate the ease of deposition at relatively low temperatures, reduced stress, and relatively low gass flow temperatures with specific reference to pages 198-201 in the text book by Wolf. Applicant neither acknowledges nor traverses this motivation on the specifics; while the examiner had given as motivation for the selection of germanium boro-phospho-silicate glass for the nonconductive oxide with second etch rate the fact that it has been known for years that germanium doping of boro-phospho-silicate glass markedly increases the etch rate (both wet and dry) of boro-phospho-silicate glass, as taught by Haller. Applicant neither acknowledges nor traverses this motivation on the specifics. Here, motivation as expressed as the reason for selection ("standard choice....because of..") obviously

means motivation for the aforementioned selections in the invention taught by the primary reference. Said motivation does not need to imply that other choices could not be made.

In conclusion with regard to the traverse of the rejection of claims 1-10 and 13 under U.S.C. 103(a), in response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the motivation stems from (a) the previously cited ease of deposition at relatively low temperatures, reduced stress, and relatively low gass flow temperatures with specific reference to pages 198-201 in the text book by Wolf, for the selection of boro-phospho silicate, and from (b) the well known fact that germanium doping of boro-phospho-silicate glass markedly increases the etch rate (both wet and dry) of boro-phospho-silicate glass, as taught by Haller.

With regard to the traverse under U.S.C. 103(a) of claim 11: the examiner notes that claim 11 defines a further limitation in which the said at least one dielectric layer comprises *one of* Si_3N_4, Ta_2O_5, *or* BST, and hence the failure in Kawakubo of the teaching of Si_3N_4 and Ta_2O_5 cited by Applicant is irrelevant. Furthermore, the purpose as cited by the examiner and as cited by Kawakubo, namely, to enhance capacitance, is

quite in parallel with the objective of enhanced storage capacity as stated by Hsia et al (cf. abstract). Hence motivation to combine the references obviously exists. The remark by Applicant that Kawakubo would "teach away" is not substantiated, nor is it even well defined. If Applicant means that Kawakubo uses the same selective etching as Hsia et al, then Applicant is referred to the further limitation of claim 11, within the context of which *this* teaching by Kawakubo is irrelevant. Parenthetically, Applicants remarks on Deboer, need to be addressed with regard to claim 11 as Deboer has not been cited by the examiner with regard to claim 11. Finally, in response to applicant's argument that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter.1985).

With regard to the traverse of the rejection under U.S.C. 103(a) of claim 12: Deboer had been cited by the examiner *only* for the Si-Ge in the conductive layer because the plurality of layers underscored by Applicant are taught by Hsia et al, as mentioned in the Office Action on page 4. The motivation by Deboer of reliability does primarily hinge on the use of silicon-germanium, as evidenced by the circumstance that either one or both electrodes can be made of silicon-germanium (see column 3, lines 29-30). Again, the two elements Ta_2O_5 and Si_3N_4 need not at all be in the cited art; this holds also for claim 12.

In overall conclusion, the examiner sees no reason to retract or otherwise modify the art rejections presented in Paper No. 4 (filed 2/14/2). Therefore, the previously made art rejections are herewith repeated in extenso.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claim 1*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Wolf et al (ISBN 0-9616721-6-1) and Haller et al (5,804,506). With reference to Figs. 6-8: Hsia et al teach a semiconductor memory device (cf. column 1, line 6 and column 4, lines 12-13) comprising:

at least one layer of a nonconductive oxide with a first etch rate 62 (cf. column 5, lines 33-35);

at least one layer of a nonconductive oxide with a second etch rate 64 (cf. column 4, line 66 – column 5, line 1);

said nonconductive oxide layer with second etching rate having a portion contacting at least a portion of said at least one layer of nonconductive oxide with first etching rate.

Hsia et al do not necessarily teach the nonconductive oxide with first etch rate to be boro-phospho silicate glass and the nonconductive oxide with second etch rate to be

germanium boro-phospho silicate glass. However, the use of boro-phospho silicate glass (BPSG) is a standard choice for the dielectric in capacitors in the semiconductor device art as evidenced by Wolf et al because of ease of deposition at relatively low temperature, reduced stress, and relatively low glass flow temperatures (pages 198-201), while it has been known for years that germanium doping of boro-phospho silicate glass markedly increases the etch rate (both wet and dry) of boro-phospho silicate glass, as witnessed by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select boro-phospho silicate glass ($B_2O_3 - P_2O_5 - S_iO_2$, hence a nonconductive oxide) for the aforementioned at least one layer 62, and to select germanium boro-phospho silicate glass (also a nonconductive oxide) for the aforementioned at least one layer 64.

3. ***Claim 2*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Wolf et al (ISBN 0-9616721-6-1) and Haller et al (5,804,506). With reference to Figs. 6-8: Hsia et al teach a semiconductor memory device (cf. column 1, line 6 and column 4, lines 12-13) comprising:

a plurality of layers of a nonconductive oxide with a first etch rate 62 (cf. column 5, lines 33-35);

a plurality of layers of a nonconductive oxide with a second etch rate 64 (cf. column 4, line 66 – column 5, line 1);

at least a portion of at least one layer of said plurality of nonconductive oxide layers with second etching rate contacting at least a portion of at least one layer of said plurality of nonconductive oxide with first etching rate (cf. Figs. 6-8).

Hsia et al do not necessarily teach the nonconductive oxide with first etch rate to be boro-phospho silicate glass and the nonconductive oxide with second etch rate to be germanium boro-phospho silicate glass. However, the use of boro-phospho silicate glass (BPSG) is a standard choice for the dielectric in capacitors in the semiconductor device art as evidenced by Wolf et al because of ease of deposition at relatively low temperature, reduced stress, and relatively low glass flow temperatures (pages 198-201), while it has been known for years that germanium doping of boro-phospho silicate glass markedly increases the etch rate (both wet and dry) of boro-phospho silicate glass, as witnessed by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select boro-phospho silicate glass ($B_2O_3 - P_2O_5 - S_iO_2$, hence a nonconductive oxide) for the aforementioned at nonconductive oxide 62, and to select germanium boro-phospho silicate glass (also a nonconductive oxide) for the aforementioned nonconductive 64.

4. ***Claim 3*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Wolf et al (ISBN 0-9616721-6-1) and Haller et al (5,804,506). With reference to Figs. 6-8: Hsia et al teach a semiconductor memory device (cf. column 1, line 6 and column 4, lines 12-13) comprising:

a plurality of layers of a nonconductive oxide (with a first etch rate) 62 (cf. column 5, lines 33-35);

a plurality of layers of a nonconductive oxide (with a second etch rate) 64 (cf. column 4, line 66 – column 5, line 1);

each layer of said plurality of layers 64 having at least a portion thereof contacting at least a portion of at least one layer of said plurality of layers 62 (cf. Figs. 6-8).

Hsia et al do not necessarily teach the nonconductive oxide layers 62 to be boro-phospho silicate glass and the nonconductive oxide layers 64 to be germanium boro-phospho silicate glass. However, the use of boro-phospho silicate glass (BPSG) is a standard choice for the dielectric in capacitors in the semiconductor device art as evidenced by Wolf et al because of ease of deposition at relatively low temperature, reduced stress, and relatively low glass flow temperatures (pages 198-201), while it has been known for years that germanium doping of boro-phospho silicate glass markedly increases the etch rate (both wet and dry) of boro-phospho silicate glass, as witnessed by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select boro-phospho silicate glass ($B_2O_3 – P_2O_5 – S_iO_2$, hence a nonconductive oxide) for the aforementioned at nonconductive oxide layers 62, and to select germanium boro-phospho silicate glass (also a nonconductive oxide) for the aforementioned nonconductive layers 64.

5. ***Claim 4*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Wolf et al (ISBN 0-9616721-6-1) and Haller et al (5,804,506). With reference to Figs. 6-8: Hsia et al teach a semiconductor memory device (cf. column 1, line 6 and column 4, lines 12-13) comprising:

at least one layer of a nonconductive oxide (with a first etch rate) 62 (cf. column 5, lines 33-35);

at least one layer of a nonconductive oxide (with a second etch rate) 64 (cf. column 4, line 66 – column 5, line 1) having at least a portion thereof contacting at least a portion of said at least one layer 62 (cf. Figs. 6-8).

Hsia et al do not necessarily teach the nonconductive oxide layers 62 to be boro-phospho silicate glass and the nonconductive oxide layers 64 to be germanium boro-phospho silicate glass. However, the use of boro-phospho silicate glass (BPSG) is a standard choice for the dielectric in capacitors in the semiconductor device art as evidenced by Wolf et al because of ease of deposition at relatively low temperature, reduced stress, and relatively low glass flow temperatures (pages 198-201), while it has been known for years that germanium doping of boro-phospho silicate glass markedly increases the etch rate (both wet and dry) of boro-phospho silicate glass, as witnessed by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select boro-phospho silicate

glass ($B_2O_3 - P_2O_5 - S_iO_2$, hence a nonconductive oxide) for the aforementioned at nonconductive oxide layers 62, and to select germanium boro-phospho silicate glass (also a nonconductive oxide) for the aforementioned nonconductive layers 64.

6. ***Claim 5*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Wolf et al (ISBN 0-9616721-6-1) and Haller et al (5,804,506). With reference to Figs. 6-8: Hsia et al teach a semiconductor memory device (cf. column 1, line 6 and column 4, lines 12-13) comprising:

a plurality of layers of a nonconductive oxide (with a first etch rate) 62 (cf. column 5, lines 33-35);

a plurality of layers of a nonconductive oxide (with a second etch rate) 64 (cf. column 4, line 66 – column 5, line 1) at least a portion of at least one layer of said plurality of layers 64 contacting at least a portion of at least one layer of said plurality of layers 62 (cf. Figs. 6-8).

Hsia et al do not necessarily teach the nonconductive oxide layers 62 to be boro-phospho silicate glass and the nonconductive oxide layers 64 to be germanium boro-phospho silicate glass. However, the use of boro-phospho silicate glass (BPSG) is a standard choice for the dielectric in capacitors in the semiconductor device art as evidenced by Wolf et al because of ease of deposition at relatively low temperature, reduced stress, and relatively low glass flow temperatures (pages 198-201), while it has been known for years that germanium doping of boro-phospho silicate glass markedly increases the etch rate (both wet and dry) of boro-phospho silicate glass, as witnessed

by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select boro-phospho silicate glass ($B_2O_3 - P_2O_5 - S_iO_2$, hence a nonconductive oxide) for the aforementioned at nonconductive oxide layers 62, and to select germanium boro-phospho silicate glass (also a nonconductive oxide) for the aforementioned nonconductive layers 64.

7. ***Claim 6*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Wolf et al (ISBN 0-9616721-6-1) and Haller et al (5,804,506). With reference to Figs. 6-8: Hsia et al teach a semiconductor memory device (cf. column 1, line 6 and column 4, lines 12-13) comprising:

a plurality of layers of a nonconductive oxide (with a first etch rate) 62 (cf. column 5, lines 33-35);

a plurality of layers of a nonconductive oxide (with a second etch rate) 64 (cf. column 4, line 66 – column 5, line 1), each layer of said plurality of layers 64 having at least a portion thereof contacting at least a portion of at least one layer of said plurality of layers 62 (cf. Figs. 6-8).

Hsia et al do not necessarily teach the nonconductive oxide layers 62 to be boro-phospho silicate glass and the nonconductive oxide layers 64 to be germanium boro-phospho silicate glass. However, the use of boro-phospho silicate glass (BPSG) is a standard choice for the dielectric in capacitors in the semiconductor device art as

evidenced by Wolf et al because of ease of deposition at relatively low temperature, reduced stress, and relatively low glass flow temperatures (pages 198-201), while it has been known for years that germanium doping of boro-phospho silicate glass markedly increases the etch rate (both wet and dry) of boro-phospho silicate glass, as witnessed by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select boro-phospho silicate glass ($B_2O_3 - P_2O_5 - S_iO_2$, hence a nonconductive oxide) for the aforementioned at nonconductive oxide layers 62, and to select germanium boro-phospho silicate glass (also a nonconductive oxide) for the aforementioned nonconductive layers 64.

8. ***Claim 7*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Wolf et al (ISBN 0-9616721-6-1) and Haller et al (5,804,506). With reference to Figs. 7 and 8: Hsia et al teach a semiconductor memory device (cf. column 1, line 6 and column 4, lines 12-13) comprising: at least one capacitor cell 78 (cf. column 6, line 47) having a portion thereof formed by at least one layer of nonconductive oxide 62 (cf. column 5, lines 33-35) and at least one layer of non-conductive oxide 64 (cf. column 4, line 66 – column 5, line 1) having at least a portion thereof contacting at least a portion of said at least one layer of nonconductive oxide 62.

Hsia et al do not necessarily teach the nonconductive oxide layers 62 to be boro-phospho silicate glass and the nonconductive oxide layers 64 to be germanium boro-

phospho silicate glass. However, the use of boro-phospho silicate glass (BPSG) is a standard choice for the dielectric in capacitors in the semiconductor device art as evidenced by Wolf et al because of ease of deposition at relatively low temperature, reduced stress, and relatively low glass flow temperatures (pages 198-201), while it has been known for years that germanium doping of boro-phospho silicate glass markedly increases the etch rate (both wet and dry) of boro-phospho silicate glass, as witnessed by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select boro-phospho silicate glass ($B_2O_3 - P_2O_5 - S_iO_2$, hence a nonconductive oxide) for the aforementioned at nonconductive oxide layers 62, and to select germanium boro-phospho silicate glass (also a nonconductive oxide) for the aforementioned nonconductive layers 64.

9. ***Claim 8*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Wolf et al (ISBN 0-9616721-6-1) and Haller et al (5,804,506). With reference to Figs. 7 and 8: Hsia et al teach a semiconductor memory device (cf. column 1, line 6 and column 4, lines 12-13) comprising: at least one capacitor cell 78 (cf. column 6, line 47) having a portion thereof formed by a plurality of layers of nonconductive oxide 62 (cf. column 5, lines 33-35) and a plurality of layers of non-conductive oxide 64 (cf. column 4, line 66 – column 5, line 1), at least a portion of at

least one layer of said plurality of layers 64 contacting at least a portion of at least one layer of said plurality of layers of nonconductive oxide 62.

Hsia et al do not necessarily teach the nonconductive oxide layers 62 to be boro-phospho silicate glass and the nonconductive oxide layers 64 to be germanium boro-phospho silicate glass. However, the use of boro-phospho silicate glass (BPSG) is a standard choice for the dielectric in capacitors in the semiconductor device art as evidenced by Wolf et al because of ease of deposition at relatively low temperature, reduced stress, and relatively low glass flow temperatures (pages 198-201), while it has been known for years that germanium doping of boro-phospho silicate glass markedly increases the etch rate (both wet and dry) of boro-phospho silicate glass, as witnessed by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select boro-phospho silicate glass ($B_2O_3 - P_2O_5 - S_iO_2$, hence a nonconductive oxide) for the aforementioned at nonconductive oxide layers 62, and to select germanium boro-phospho silicate glass (also a nonconductive oxide) for the aforementioned nonconductive layers 64.

10. ***Claims 9, 10 and 13*** *are rejected* under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Wolf et al (ISBN 0-9616721-6-1) and Haller et al (5,804,506). With reference to Figs. 7 and 8: Hsia et al teach a semiconductor memory device (cf. column 1, line 6 and column 4, lines 12-13) comprising: at least one

capacitor cell 78 (cf. column 6, line 47) having a portion thereof formed by a plurality of layers of nonconductive oxide 62 (cf. column 5, lines 33-35) and a plurality of layers of non-conductive oxide 64 (cf. column 4, line 66 – column 5, line 1), each layer of 64 having at least a portion thereof contacting at least a portion thereof contacting of at least one layer of said plurality of layers 64 contacting at least a portion of at least one layer of said plurality of layers 62.

Hsia et al do not necessarily teach the nonconductive oxide layers 62 to be boro-phospho silicate glass and the nonconductive oxide layers 64 to be germanium boro-phospho silicate glass. However, the use of boro-phospho silicate glass (BPSG) is a standard choice for the dielectric in capacitors in the semiconductor device art as evidenced by Wolf et al because of ease of deposition at relatively low temperature, reduced stress, and relatively low glass flow temperatures (pages 198-201), while it has been known for years that germanium doping of boro-phospho silicate glass markedly increases the etch rate (both wet and dry) of boro-phospho silicate glass, as witnessed by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select boro-phospho silicate glass ($B_2O_3 – P_2O_5 – S_iO_2$, hence a nonconductive oxide) for the aforementioned at nonconductive oxide layers 62, and to select germanium boro-phospho silicate glass (also a nonconductive oxide) for the aforementioned nonconductive layers 64.

With regard to claim 10: the semiconductor memory device taught by Hsia et al further comprises at least one dielectric layer (cf. column 7, line 5) and a conductive layer (cf. column 7, line 4) over said at least one dielectric layer ("over said" is not taught verbatim but examiner takes official notice that this is obvious in the art of capacitors generally and in the art of semiconductor memory device capacitors in particular, in the sense that otherwise one would not have a capacitor).

With regard to claim 13: the semiconductor memory device of Hsia et al further comprises at least one dielectric layer covering at least portions of said plurality of layers 62 and 64; and a conductive layer covering at least a portion of said dielectric layer (cf. column 7, lines 4-6).

11. ***Claim 11*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Hsia et al, Wolf et al, and Haller et al as applied to claim 10 above, and further in view of Kawakubo (5,889,696). As detailed above, claim 10 (on which claim 11 depends) is unpatentable over Hsia et al in view of Wolf et al and Haller et al, neither of whom, however, specifically teach the semiconductor memory device of claim 10 with the further limitation as defined by claim 11.

However, particularly the use of BST as a high dielectric in capacitors in semiconductor memory devices has long been taught as a means to increase the charge storage capacity of capacitors, as witnessed, for example, by Kawakubo et al, who teach a semiconductor memory device (cf. Abstract, first sentence) with capacitor (cf. Abstract, first sentence) *for the very purpose of achieving very high charge storage*

ability through the very high dielectric constant of BST (cf. column 9, lines 58-63). *Therefore, it would have been obvious* to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to include the further limitation of claim 11.

12. ***Claim 12*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Hsia et al, Wolf et al, and Haller et al as applied to claim 10 above, and further in view of De Boer et al (5,930,106 and DERWENT copy, under "Novelty"). As detailed above, claim 10 (on which claim 12 depends) is unpatentable over Hsia et al in view of Wolf et al and Haller et al, who, however, do not specifically teach the conductive layer to comprise Si-Ge.

However, Si-Ge has long been taught as semiconductor memory device capacitor electrode material for the purpose of high reliability, as evidenced by De Boer et al, who teach a Si-Ge capacitor plate for the purpose of achieving high reliability (cf. particularly the DERWENT SUMMARY of De Boer et al) in a semiconductor memory device capacitor (cf. Abstract, final sentence; column 2, lines 24-28). Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention of Hsia et al at the time it was made so as to include the further limitation of claim 12.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
June 22, 2002

NATHAN J. FLYNN
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